SUBSTRATES BONDED WITH OXIDE AFFINITY AGENT AND BONDING METHOD

FIELD OF THE INVENTION

[0001] The present invention relates to bonded substrates, and is more particularly related to bonding substrates with a bonding material that includes an oxide affinity material.

BACKGROUND OF THE INVENTION

[0002] In large scale integration, electrical devices such as complementary metal-oxide semiconductor (CMOS) circuitry are fabricated in large qualities on substrates. These substrates can be bonded together using microfabrication techniques to efficiently manufacture micromachined structures. The term "semiconductor substrate" includes semiconductive material. The term is not limited to bulk semiconductive material, such as a silicon wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term "substrate" refers to any supporting structure including but not limited to the semiconductor substrates described above. A substrate may be made of silicon, glass, gallium arsenide, silicon on sapphire (SOS), epitaxial formations, germanium, germanium silicon, diamond, silicon on insulator (SOI) material,

selective implantation of oxygen (SIMOX) substrates, and/or like substrate materials. Preferably, the substrate is made of silicon, which is typically single crystalline.

[0003] In some bonding applications, the substrates that are bonded together are semiconductor substrates such as silicon wafers. In wafer bonding, two or more wafers are bonded together each of which can have a plurality of electrical devices formed thereon prior to the wafer bonding process. The bonding process typically forms a controlled environment, such as a hermetic seal, between adjacent wafers. After the wafers are bonded together, they can be are singulated into individual dice, either before or after packaging.

[0004] During the fabrication process for each wafer, a native oxide can form on an exposed surface of the wafer. This native oxide can weaken the bond that is formed with another wafer during the bonding process. Native oxide also prevents a uniform bond from forming between adjacent wafers. In order to avoid the native oxide problem, the native oxide is removed using mechanical or ultrasonic scrubbing of the wafer surface. These scrubbing processes are useful only when the bond between surfaces on adjacent wafers do not require precise alignment and are not distributed over an extended area on adjacent wafers. As such, mechanical and ultrasonic scrubbing for native oxide removal is of limited use.

[0005] Reverse sputtering can also be used to remove native oxide from substrate surfaces immediately prior to bonding to another substrate. It is desirable to fabricate chips with as few processes and in as short of time in a clean room environment as practical. Short processing time in the clean room

environment is desirable because operation and maintenance of the clean room environment for chip fabrication using semiconductor technology processes is time consuming and expensive. Fewer processes in chip fabrication are desirable because each fabrication process is both an expense and an opportunity to reduce yield. Moreover, the extra step of reverse sputtering tends to decrease yield, require additional fabrication tools, and generally adds cost to the wafer bonding process.

[0006] Another way to remove native oxide prior to wafer bonding is to etch the native oxide. For example, a silicon surface can be etched to remove its native oxide prior to a noble metal deposition, such as gold, that will be used to form a gold-silicon diffusion bond to another silicon wafer. Variability in the native oxide thickness, which may grow in the time between the etch and a subsequent process step or due to other environmental factors, could increase the variability in the bond between adjacent wafers, thus preventing a uniform bond from forming.

[0007] It would be an advance in the art to provide a uniform bond between adjacent substrates by removal of native oxide from the bonding surfaces there between.

SUMMARY OF THE INVENTION

[0008] An electrical device has first and second substrates bonded together with a first material. Dispersed within the first material is a reducing agent for the diffusion therein of oxidation of a second material of which at least one of the first and second substrates is composed. The reducing agent has a higher affinity for oxygen than that of the second material.

[0009] These and other features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

DESCRIPTION OF THE DRAWINGS

[0010] To further clarify the above and other advantages and features of the present invention, a more particular description of the invention will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. The same numbers are used throughout the drawings to reference like features and components. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[0011] Figure 1 is a cross-sectional view of an embodiment of the invention depicting a cut away section of two wafers to be bonded together by a bonding layer adhered to one of the wafers, where the other wafer has a native oxide thereon;

[0012] Figure 2 is a cross-sectional view of the structure seen in Figure 1 after further processing, where a wafer bonding process has removed a portion of the native oxide where the wafers are bonded together.

[0013] Figure 3 depicts a flow chart illustrating a bonding process that can be used to fabricate the structures seen in Figures 1-2;

[0014] Figure 4 is a cross-sectional view of an embodiment of the invention depicting a cut away section of two wafers to be bonded together by a bonding

layer adhered to one of the wafers, where the other wafer has thereon a silicon layer having a native oxide thereon;

[0015] Figure 5 is a cross-sectional view of the structure seen in Figure 4 after further processing, where a wafer bonding process has removed a portion of the native oxide where the wafers are bonded together.

[0016] Figure 6 depicts a flow chart illustrating a bonding process that can be used to fabricate the structures seen in Figures 4-5;

[0017] Figure 7 is a cross-sectional view of another embodiment of the invention depicting a cut away section of two wafers to be bonded together by a triple film stack, where the triple film stack includes an oxide affinity agent layer between two layers of noble metal, where one of the wafers has a native oxide thereon;

[0018] Figure 8 is a cross-sectional view of the structure seen in Figure 7 after further processing, where a wafer bonding process has removed the native oxide where the wafers are bonded together.

[0019] Figure 9 depicts a flow chart illustrating a bonding process that can be used to fabricate the structures seen in Figures 7-8.

[0020] Figure 10 is a cross-sectional view of an embodiment of the invention depicting a cut away section of two wafers to be bonded together by a triple film stack of an oxide affinity agent layer between two layers of noble metal, where one of the wafers has thereon a silicon layer having a native oxide thereon;

[0021] Figure 11 is a cross-sectional view of the structure seen in Figure 10 after further processing, where a wafer bonding process has removed the native oxide where the wafers are bonded together.

[0022] Figure 12 depicts a flow chart illustrating a bonding process that can be used to fabricate the structures seen in Figures 10-11.

[0023] Figure 13 depicts a pair of portions of a respective pair of semiconductor wafers, each having a plurality of electrically insulated integrated circuits fabricated there between, where the portions are bonded together by a bonding structure that forms a closed environment between the portions, and where the portions were formed by scribing and singulating the respective wafers to form individual die for packaging.

DETAILED DESCRIPTION

[0024] The present invention disperses in a bonding material a reducing agent capable of removing oxidation on surfaces to be bonded together such that the oxidation can be removed during the bonding process. When a native oxide is formed upon a surface that is to be joined to another surface, it is desirable to remove the native oxide in order to form a strong and uniform bond to the other surface. By dispersing a reducing agent in a bonding material and then placing the bonding material in contact with the native oxide in a bonding process, the native oxide will be removed. The removal of the native oxide occurs because the agent has a higher affinity for oxygen than the underlying material upon which the native oxide has formed. The agent in the bonding material greatly increases the driving force for the removal of the native oxide, thus enabling a uniform bond between surfaces to be joined together. As the bonding process proceeds at an elevated temperature, the oxygen in the native oxide will diffuse into the bulk of the bonding material. With the agent dispersed in the bonding material, the

oxygen will preferentially combine with the agent so as to remove the native oxide at an increased rate.

[0025] In silicon wafer bonding, where one silicon wafer is bonded to another silicon wafer, it is desirable to remove native oxide, in any degree of thickness, from both wafer surfaces that are to form an interface there between. One material that can be used to bond the wafers together is gold. It is preferable to co-deposit an agent with the gold so as to remove the native oxide from one or both interface surfaces of the wafers. The free energy of formation of silicon dioxide is recognized as being in a range from about -200 Kcal/mol to about -205 Kcal/mol. As such, the agent in the bonding material should have a higher oxygen affinity than silicon, meaning that the free energy of formation must be more negative than either gold or silicon dioxide, or less than a range from about -200 Kcal/mol to about -205 Kcal/mol. The oxide of the agent is therefore more stable than silicon dioxide.

[0026] Figures 1-2 show views of a structure 100 in electrical devices that can be formed using microfabrication techniques. Two (2) substrates are seen in structure 100. By way of example, each substrate can be a wafer composed of a semiconductor material such as silicon. Figure 1 shows a wafer 102 to be bonded to a wafer 104. Each wafer 102, 104 may include other layers and/or circuitry not shown for simplicity in order to implement other various functionalities. As seen in Figure 1, circuitry 110 is fabricated on each wafer 102, 104. Circuitry 110 can include microcircuitry such as CMOS components.

[0027] In a preferred embodiment of the invention, wafers 102, 104 have an insulator 112 deposited and patterned over circuitry 110 on each wafer 102, 104.

Insulator 112 may be comprised of any suitable insulating material known in the art, including but not limited to a wet or dry silicon dioxide (SiO_2), a nitride material including silicon nitride, tetraethylorthosilicate ($Si\text{-}OC_2H_5)_4$) (TEOS) based oxides, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), oxide-nitride-oxide (ONO), polyamide film, tantalum pentoxide (Ta_2O_5), plasma enhanced silicon nitride ($P\text{-}SiN_x$), titanium oxide, oxynitride, germanium oxide, a spin on glass (SOG), any chemical vapor deposited (CVD) dielectric including a deposited oxide, a grown oxide, and /or like dielectric materials.

[0028] A native oxide 124 forms upon wafer 104 due to environmental conditions. A bonding layer 114 is formed on wafer 102 and is preferably composed of an alloy that is formed by a physical vapor deposition process (PVD) using a powdered target or a target composed of an alloy. Bonding layer 114 can be formed so as to be patterned, such as by use of an etch process in combination with directional sputtering, a deposition mask, a collimator, or combinations thereof. The thickness of bonding layer 114 is preferably in a range from about 50 Angstroms to about 20,000 Angstroms. Since the material of which bonding layer 114 is composed is capable of conducting current, bonding layer 114 can be used as an electrical connection between circuitry 110 included within wafers 102, 104. The PVD process preferably co-sputters a noble metal, such as gold or a gold alloy, with a reducing agent that has a higher affinity for oxygen than does the material of which wafer 104 is composed. As used herein, a noble metal is intended to mean any of several metallic chemical elements that have outstanding resistance to oxidation, even at high temperatures. These metallic

chemical elements include rhenium, ruthenium, rhodium, palladium, silver, osmium, iridium, platinum, and gold, and are more particularly characterized as the metals of groups VIIb, VIII, and Ib of the second and third transition series of the periodic table.

[0029] The result of the co-sputtering process is the formation of an alloy of which bonding layer 114 is composed. By way of example, when wafer 104 is composed of silicon, and the noble metal is gold or a gold alloy, the agent that is co-sputtered and thereby alloyed with the gold or gold alloy can be Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, Zr, or alloy thereof, with the PVD process being conducted in a temperature range from about 100 degrees Centigrade to about 1000 degrees Centigrade. More preferably, the noble metal will be gold and the co-sputtered material will be Ti Al, Li, Mg, Ca, or an alloy thereof, with the PVD process being conducted in a temperature range from about 100 degrees Centigrade to about 1000 degrees Centigrade. Preferably, the material that is co-sputtered with the noble metal will be less than about half of the weight of bonding layer 114 and will have a free energy that is lower than that of silicon dioxide or lower than a range that is from about -200 Kcal/mol to about -205 Kcal/mol.

[0030] Following the PVD process, bonding layer 114 is patterned as seen in Figure 1. Wafers 102, 104 are pressed together with bonding layer 114 there between. The bonding together of wafers 102, 104 may be of any suitable configuration as long as the bonding materials can be bonded at compatible temperatures for microcircuitry fabrication applications. The bonding process, which can be an annealing process, causes bonding layer 114 to form a bond

between wafers 102, 104 to create the single structure 100 seen in Figure 2. When wafers 102, 104 are bonded together by bonding layer 114 as seen in Figure 2, a region having a closed environment and/or a hermetic sealed region can thereby be formed between wafers 102, 104. An example of the formation of a closed environment is seen in Figure 13 where a structure 500 has a bonding structure 130 that bonds wafers 102, 104 together to form a closed environment 132 there between. Bonding structure 130 forms a seal between wafers 102, 104. As such, circuits 110, which are electrically insolated within insulator 112 on both of wafers 102, 104, are within closed environment 132.

[0031] A bond is "sufficient" for the purposes of the present invention when it is capable of maintaining an alignment of wafer 102 with respect to wafer 104 during normal operation of the structure 100. As such, after the bonding process, the bond should be sufficient to keep wafer 102 attached and aligned to wafer 104 as well being configured to form an electrical connection between the integrated circuits 110 in wafer 102 and the integrated circuits 110 in wafer 104.

[0032] In the bonding process, wafers 102, 104 are preferably pressed together at a pressure of about 10 KPa to about 300 MPa to form a bond between wafer 104 and bonding layer 114 of wafer 102. An annealing chamber can be used to accomplish the bonding process. Although not necessary for implementing the invention, it may be preferable to change or "ramp" the temperature. Preferably, the bonding or annealing temperature of the bonding process will be at or below approximately 450 degrees Celsius. By keeping temperatures of the bonding or annealing process below approximately 450 degrees Celsius, any CMOS circuitry included in either of the wafers 102, 104 should not be damaged. Figure 2

reflects the absence of native oxide 124 where bonding layer 114 has made contact therewith. Native oxide 124 is removed by diffusion into bonding layer 114. Included in bonding layer 114 is noble metal and an oxide affinity material that is dispersed within the noble metal of bonding layer 114. The oxide affinity material reacts with the native oxide.

[0033] Figure 3 is a flow chart showing a process 300 for fabricating structure 100 seen in Figures 1-2. Structure 100 is an electrical device made by bonding surfaces together with a material having dispersed therein a reducing agent into which oxidation on the surfaces is diffused to remove the oxidation while bonding. In accordance with the flow chart seen in Figure 3, at step 302 integrated circuits (ICs) are fabricated on a plurality of substrates, each of which may be wafers 102, 104. At step 304 an insulator is deposited and patterned over the ICs, such as is seen in Figure 1 at reference numeral 112 on each of wafers 102, 104. At step 308 a reducing agent is co-sputtered with a noble metal upon one of the wafers. At step 310, the co-sputtered layer is patterned to form a bonding layer 114 seen in Figure 1. The wafers are bonded at step 312 in a bonding process that removes a portion of a native oxide where the patterned co-sputtered layer contacts the other wafer, as seen in structure 100 seen in Figure 2. One skilled in the art should realize that a variety of temperatures, times, and pressures are possible for the bonding process depicted by Figure 3.

[0034] Another embodiment of the invention is depicted in Figures 4-5 where a structure 200 is fabricated using a process 600 of Figure 6. Figures 4-5 differ from Figures 1-2 in that native oxide region 124 is upon silicon layer 126 on wafer 104. Silicon layer 126 is preferably formed by plasma enhanced chemical vapor

deposition (PECVD) and is subsequently patterned as seen in structure 200 of Figure 4. As seen in Figure 5, bonding layer 114 on wafer 102 is bonded to PECVD silicon layer 126 on wafer 104. During the bonding of wafers 102, 104, there is a removal of a portion of native oxide layer 124 on silicon layer 126 as seen in Figure 5. As such, the removed portion of native oxide layer 124 diffuses into bonding layer 114, and bonding layer 114 bonds to PECVD silicon layer 126 so as to form structure 200 as seen in corresponding Figure 5. Process 600 in Figure 6 is similar to process 300 in Figure 3 with the addition of step 605 that deposits and patterns the PECVD silicon layer 126. Structure 200 of Figures 4-5 thereby can be used to form closed environment 132 as seen in Figure 13.

[0035] Another embodiment of the invention is depicted in Figures 7-8 which differ from Figures 1-2 in that bonding layer 114 of structure 100 is replaced with a triple film stack in structure 300. Like bonding layer 114 of structure 100, the triple film stack of structure 100 is adhered to wafer 102. The triple film stack is used to bond surfaces together and has a reducing agent into which oxidation is diffused to remove the oxidation while bonding. In Figure 7, the triple film stack includes a noble metal trace 116. Noble metal trace 116 is preferably composed of gold or an alloy thereof, and can be formed by conventional deposition techniques which will preferably be a PVD process. An agent layer 118 is formed upon noble metal trace 116 and will preferably having a thickness in a range from about 0.1 microns to not more than about 2 microns. Agent layer 118 will preferably be formed by sputtering a target composed of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, Zr, or an alloy thereof, with the PVD process being conducted in a temperature range

from about 100 degrees Centigrade to about 1000 degrees Centigrade. More preferably, when noble metal trace 116 is composed of gold, then the agent layer 118 will be composed of Ti Al, Li, Mg, Ca, or an alloy thereof.

[0036] A noble metal cap 120, preferably composed of gold or an alloy thereof, is seen in Figures 7-8 as being formed upon agent layer 118. Noble metal cap 120 will preferably have a thickness of less than about 2 microns and most preferably in a range from about 50 Angstroms to about 100 Angstroms. Noble metal cap 120 will preferably be continuous upon agent layer 118 and will be formed using conventional deposition equipment. Noble metal cap 120 prevents agent layer 118 from reacting with gases in the ambient. Preferably, agent layer 118 will form a composite structure with both noble metal trace 116 and noble metal cap 120 prior to or during a process that bonds wafers 102, 104 together.

[0037] After noble metal cap 120 is formed, a patterning of noble metal trace 116, agent layer 118, and noble metal cap 120 takes place to form the representation thereof seen in Figures 7-8.

[0038] Figure 8 shows wafers 102, 104 being pressed together with the patterned noble metal trace 116, agent layer 118, noble metal cap 120 there between. Wafer 102 is bonded to wafer 104 similar to the bonding process described above with respect to Figures 1-3, and during which a top of native oxide 124 is removed from an exposed surface of wafer 104. Particularly, noble metal cap 120 is brought into contact with native oxide 124 on wafer 104 under pressure and elevated temperature in the bonding process, as particularly depicted in the process steps seen in Figure 9 which are discussed below.

[0039] Substrate bonding process 900 is illustrated in a flow chart seen in Figure 9, where the bonding process 900 corresponds to the structure 300 depicted in Figures 7-8. In accordance with the flow chart seen in Figure 9, at step 902 integrated circuits (ICs) are fabricated on a plurality of substrates, each of which may be silicon wafer. At step 904 an insulator is deposited and patterned over the ICs, such as is seen in Figures 7-8 at reference numeral 112. At step 906, a noble metal base is formed. At step 908, a reducing agent is formed upon the noble metal base. At step 910, a noble cap is formed on the reducing agent. The noble metal base, the reducing agent, and the noble metal cap are all patterned at step 912. The substrates are bonded together at step 914 as seen in Figure 8 so as to form a closed environment and/or a hermetic seal between wafers 102, 104, similar to that seen in Figure 13. As seen in structure 300 in Figure 8, a portion of native oxide 124 is removed from wafer 104 where patterned metal cap 120 contacts wafer 104 during the wafer bonding process.

[0040] Another embodiment of the invention is depicted in Figures 10-11 where a structure 400 is fabricated using a process 1200 of Figure 12. Figures 10-11 differ from Figures 7-8 in that native oxide region 124 is upon silicon layer 126 on wafer 104. Silicon layer 126 is formed by plasma enhanced chemical vapor deposition (PECVD) and is subsequently patterned as seen in structure 400 of Figures 10-11. As seen in Figure 11, noble metal cap 120 on wafer 102 is bonded to silicon layer 126 on wafer 104 during which there is a removal of a portion of the top native oxide layer 124. As such, the removed portion of the top native oxide layer 124 diffuses into noble metal cap 120 and noble metal cap 120 bonds to silicon layer 126 to form structure 400 as seen in corresponding Figure

11. Process 1200 in Figure 12 is similar to process 900 in Figure 9 which the addition of step 1205 that deposits and patterns the PECVD silicon layer 126. Structure 400 of Figures 10-11 thereby can be used to form closed environment 132 as seen in Figure 13.

[0041] Following each bonding process 300, 600, 900, and 1200 in Figures 3, 6, 9, and 12, respectively, the bonded substrates can be scribed and singulated to form individual die. Each die can be packaged before or after the singulation process so as to contain there within a closed environment and/or a hermetic seal.

[0042] The embodiments of the invention disclosed herein for forming bonded wafer structures, and packaged die therefrom, can be fabricated using known process equipment in a semiconductor fabrication operation and can allow for a broad range of materials and dimensions for said structures. It should be recognized that, in addition to the bonded substrate embodiments of the invention that are described above, this invention is also applicable to alternative bonded structure technologies in electrical devices, such as a die that encapsulates a closed environment or hermetically sealed atmosphere, MicroElectroMechanical Systems (MEMS), air bags applications, field emitter display devices, accelerometers, bolometers, mirror arrays, optical switches, pressure gauges, turbine chambers, combustion chambers, and multiple wafers memory devices such as are used for Atomic Resolution Storage (ARS) and the like.

[0043] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The

scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.